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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,116	08/29/2000	James D. Barnette	BARNETTE 2-2	2342

27964 7590 04/21/2004

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	**PAPER NUMBER**
2631	8

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,116	BARNETTE ET AL.	
	Examiner	Art Unit	
	Qutub Ghulamali	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-27* is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. This Office Action is responsive to the Amendment filed on 01/30/2004.

Response to Arguments

2. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

The rejection (s) based on newly discovered art follows.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paulos et al ("Paulos") (US Patent 6,208,671) in view of Yang (US Patent 6,573,940, new art).

Consider claims 1, 8, Paulos teaches a resampler (figs. 2-5), a sample rate converter comprising an interpolation filter, coupled to a resampler 302, configured to receive a 1-bit serial data stream with a data rate 64Fs1 from incoming AES frames (col. 6, lines 1-13), the upsampler 401 upsample the rate Fs1 of input signal A by a factor of two (2) (Plurality is

generally regarded by Office as two or more samples), and a decimator connected together, the interpolation filter 301, composed of an upsampler 401, filter 402, upsampler 403, etc., resampler 302 consists of linear interpolator 502, rate estimator 503, and quantizer 504, 502 is designed to transform input signal B to signal C (equation 2), where B(n) is the value of signal B at the sample time n=0, 1, 2, 3, B(n+1) is the value of signal B at the immediate following sample time (n+1), T1 is the sample period corresponding to sample rate UF.sub.s1, T2 is the sample period corresponding to sample rate 128F.sub.s2, and a(n) is the relative phase between B(n) and B(n+1), the output of receiver 204, as well as the output of serial audio input circuit 201, are provided to clock & data recovery circuit 205, to recover a high-frequency, low-jitter RMCK, given a low frequency input clock, such function is achieved with a phase-locked loop (PLL) (not shown), the low frequency input can either be the F.sub.s1 ILRCK, or a clock derived from the biphase-mark data of receiver 204, the interpolation filter receives as input the signal A (n) having a first sample rate, the interpolation filter unsamples the sample rate of the sample to a sample rate Ufs1, where the variable upsampling factor U is directly related to the ratio of Fs_2/Fs_1, the interpolation filter then performs interpolation between samples values of the signal, and provides an output (col.. 5, lines 64-67; col. 6, lines 1-13; col. 8, lines 13-44, 50-60). Paulos however, does not disclose samples selected as interpolated samples wherein the selection stage is configured to select one of a plurality of intermediate samples to provide output sample that corresponds to a phase of oscillator. Yang discloses a rate converter configured to receive and resample input data samples to generate resampled video samples the first sample including a plurality of selector elements wherein each processed data sample is generated by delaying an input sample by zero or more clock cycles to correspond to a phase of

the clock, the selected processed data samples from the sets, which are associated with a particular phase to be interpolated are combined to generate an output sample. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Paulos's sample rate converter to include a plurality of selector elements wherein each processed data sample is generated by delaying an input sample by zero or more clock cycles so as to correspond to a phase of the clock as taught by Yang (col. 26, lines 27-46).

Regarding claims 2, 3, 9, 10, Paulos et al teaches a resampler (figs. 2-5), a sample rate converter comprising an interpolation filter, coupled to a resampler 302, configured to receive a 1-bit serial data stream with a data rate 64Fs1 from incoming AES frames (col. 6, lines 1-13), the upsampler 401 upsample the rate Fs1 of input signal A by a factor of two (2) (Plurality is generally regarded by Office as two or more samples), and a decimator connected together, the interpolation filter 301, composed of an upsampler 401, filter 402, upsampler 403, etc., resampler 302 consists of linear interpolator 502, rate estimator 503, and quantizer 504, 502 is designed to transform input signal B to signal C (equation 2), where B(n) is the value of signal B at the sample time n=0, 1, 2, 3, B(n+1) is the value of signal B at the immediate following sample time (n+1), T1 is the sample period corresponding to sample rate UF.sub.s1, T2 is the sample period corresponding to sample rate 128F.sub.s2, and a(n) is the relative phase between B(n) and B(n+1), the output of receiver 204, as well as the output of serial audio input circuit 201, are provided to clock & data recovery circuit 205, to recover a high-frequency, low-jitter RMCK, given a low frequency input clock, such function is achieved with a phase-locked loop (PLL) (not shown), the low frequency input can either be the F.sub.s1 ILRCK, or a clock derived from the biphase-mark data of receiver 204, the interpolation filter receives as input the

signal A (n) having a first sample rate, the interpolation filter unsamples the sample rate of the sample to a sample rate Ufs1, where the variable upsampling factor U is directly related to the ratio of Fs_2/Fs_1, the interpolation filter then performs interpolation between samples values of the signal, and provides an output (col.. 5, lines 64-67; col. 6, lines 1-13; col. 8, lines 13-44, 50-60).

Regarding claims 4 and 11 Paulos discloses adders (figs. 11, 12) resampler comprising of a first adder receiving as input a constant value one (1) and the output signal from the delay circuit, the first adder calculating the sum of the inputs, the first adder providing the sum as an output; a second adder receiving as input the output of the first adder and a negative T1/T2 value, the second adder calculating a sum of the inputs, the second adder providing the sum as an output; and a comparator receiving as input the output of the first adder and the T1/T2 value, the comparator outputting a HIGH INCR signal if the output of the first adder is greater than the positive T1/T2 value, the comparator outputting a LOW INCR signal if the output of the first adder is less than the positive T1/T2 value (col. 16, lines 53-64).

Regarding claims 5 and 12, Paulos discloses (fig. 4) resampler comprising filters 402, 404 configured to filter output of upsampler 401 (col. 8, lines 13-30).

With reference to claims 6 and 13, Paulos discloses resampler comprising of multiple filter section 1302 to further reduce the aliases and images in the baseband region (col. 14, lines19-24).

Regarding claim 7 and 14, Paulos discloses resampler consists of a delay circuit 1105 (figs. 11, 12) as part of the linear interpolator section (col. 11, lines 54-65).

Allowable Subject Matter

5. Claims 15-27 allowed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dholakia et al (US Patent 6,389,064), Christopher et al (US Patent 5,351,087), Peeters et al (US Patent 6,628,738) and Ma et al (US Patent 5,748,126) are cited as arts of reference.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (703) 305-7868. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 703 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
April 16, 2004.

M. Ghayour

MOHAMMAD H. GHAYOUR
PRIMARY EXAMINER